NTQS6466

Product Preview

Power MOSFET 6.8 Amps, 20 Volts N-Channel TSSOP-8

Features

- New Low Profile TSSOP-8 Package
- Ultra Low R_{DS(on)}
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- IDSS and VDS(on) Specified at Elevated Temperatures

Applications

- Power Management in Portable and Battery–Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular and Cordless Telephones
- Lithium Ion Battery Applications
- Note Book PC

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	10 secs	Steady State	Unit			
VDS	2	0	Vdc			
VGS	1	2				
۱D	8.1 6.6	6.8 5.4	Adc			
IDM	±30				Apk	
IS	1.35	0.95	Adc			
PD	1.5 1.0	1.05 0.67	W			
Тј, Т _{stg}	-55 to +150		°C			
E _{AS}	1.36		J			
	V _{DS} V _{GS} ID IDM IS PD TJ, T _{stg}	VDS 2 VGS 1 ID 8.1 6.6 1 IDM ± IS 1.35 PD 1.5 1.0 1.5 TJ, Tstg -55 to EAS 1.3	secs State VDS 20 VGS 12 ID 8.1 6.6 5.4 IDM ±30 IS 1.35 PD 1.5 1.0 0.67 TJ, Tstg -55 to +150 EAS 1.36			

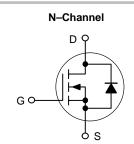
1. Surface mounted to 1" x 1" FR-4 board.

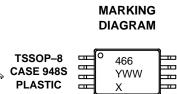


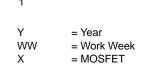
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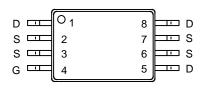
6.8 AMPERES 20 VOLTS RDS(on) = 17 mΩ







PIN ASSIGNMENT



Top View

ORDERING INFORMATION

Device	Package	Shipping
NTQS6466	TSSOP-8	100 Units/Rail
NTQS6466R2	TSSOP-8	3000/Tape & Reel

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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THERMAL RESISTANCE RATINGS

Rating	Symbol	Typical	Max	Unit
Maximum Junction-to-Ambient (Note 2.)	R _{0JA}			°C/W
t ≤ 10 sec		65	83	
Steady State		100	120	
Maximum Junction-to-Foot	R _{0JF}			°C/W
Steady State		43	52	

ELECTRICAL CHARACTERISTICS (T_J = 25° C unless otherwise noted)

Characteristic		Symbol	Min	Тур	Max	Unit
STATIC						

STATIC					
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = 250 \mu A)$	V _{GS(th)}	0.45	0.9	-	Vdc
Gate–Body Leakage ($V_{DS} = 0 \text{ Vdc}, V_{GS} = \pm 8 \text{ Vdc}$)	IGSS	-	-	±100	nAdc
Zero Gate Threshold Voltage Drain Current ($V_{DS} = 16 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}$) ($V_{DS} = 16 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, T_{J} = 70^{\circ}\text{C}$)	IDSS			1.0 10	μAdc
On–State Drain Current (Note 3.) (V _{DS} = 5.0 Vdc, V _{GS} = 4.5 Vdc)	I _{D(on)}	20	-	-	Adc
$ Drain-Source On-State Resistance (Note 3.) \\ (V_{GS} = 4.5 Vdc, I_D = 8.1 Adc) \\ (V_{GS} = 2.5 Vdc, I_D = 6.6 Adc) $	R _{DS(on)}		0.014 0.017	0.017 0.020	Ω
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 8.1 Adc) (Note 3.)	9FS	-	30	-	S
Diode Forward Voltage ($I_S = 1.35$ Adc, $V_{GS} = 0$ Vdc (Note 3.)	V _{SD}	-	0.65	1.1	Vdc

DYNAMIC (Note 4.)

Total Gate Charge	(V _{DS} = 10 Vdc,	Qg	-	25	27	nC
Gate-Source Charge	$V_{GS} = 5.0 \text{ Vdc},$	Qgs	-	3.2	-	
Gate–Drain Charge	I _D = 8.1 Adc)	Q _{gd}	-	7.0	-	
Turn–On Delay Time	(//= =	^t d(on)	-	17	45	ns
Rise Time	$(V_{DD} = 10 \text{ Vdc}, \text{ R}_{L} = 10 \Omega,$ $I_{D} \cong 1.0 \text{ Adc},$	tr	-	80	100	
Turn-Off Delay Time	V _{GEN} = 4.5 Vdc, R _G = 6.0 Ω)	^t d(off)	-	95	110	
Fall Time	- (G = 0.0.22)	tf	-	90	100	
Source–Drain Reverse Recovery Time	(I _F = 1.5 Adc, di/dt = 100 A/μs)	t _{rr}	-	28	70	ns

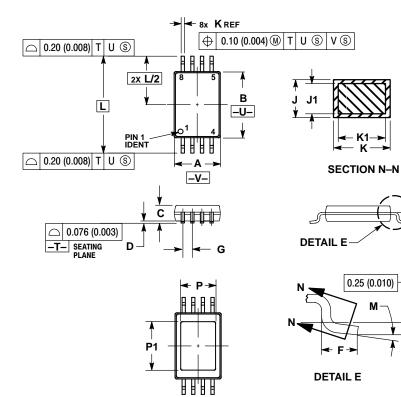
2. Surface mounted to 1" x 1" FR-4 board.

3. Pulse Test: Pulse Width \leq 300 µs, Duty Cycle \leq 2%.

4. Guaranteed by design, not subject to production testing.

PACKAGE DIMENSIONS





-W-

- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH.
 PROTRUSIONS OR GATE BURRS. MOLD FLASH.
 OR GATE BURRS SHALL NOT EXCEED 0.15
- On GATE DORS OF A STATE OF A ST
- PER SIDE. 5. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	2.90	3.10	0.114	0.122
В	4.30	4.50	0.169	0.177
C		1.10		0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65	0.65 BSC		BSC
ſ	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40		0.252 BSC	
Μ	0°	8°	0°	8 °
Ρ		2.20		0.087
P1		3.20		0.126

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JAPAN: ON Semiconductor, Japan Customer Focus Center 4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031 Phone: 81–3–5740–2700 Email: r14525@onsemi.com

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